Project Title

Group Number
Group Members

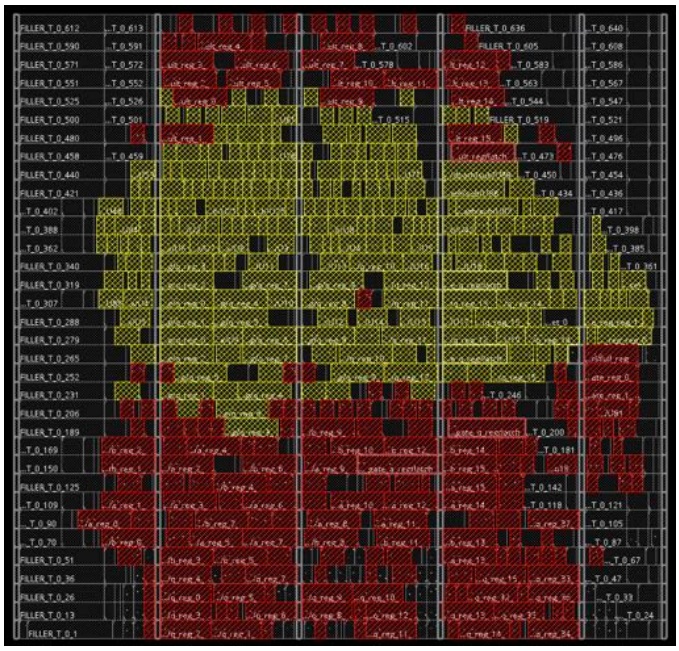
1. Evaluation

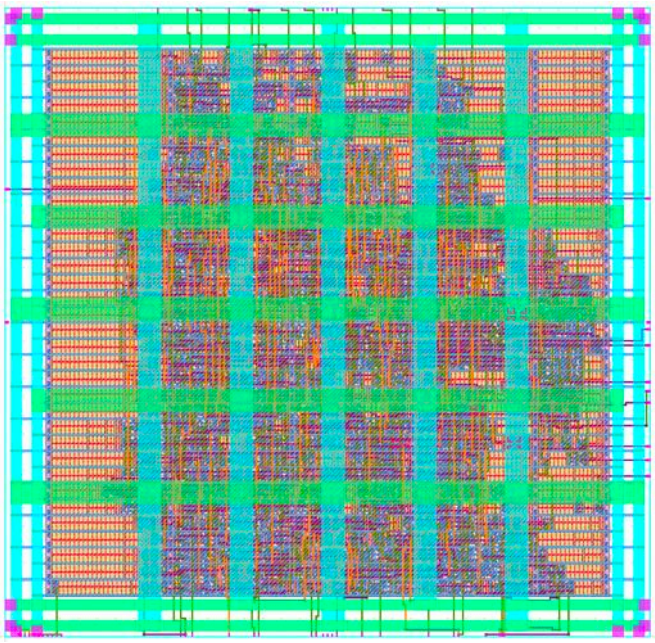
Use 10-point times or palantino font, single-spaced, with 1" margins. Include 1-2 pages of text discussing your current evaluation results.

Start with a discussion of your accelerator block-level results. Do not just mention the total area, cycle time, and power. Be sure to dive into the results to discuss the detailed area break-down, where the critical path goes, and the detailed power break-down.

Then do a comparative analysis of your processor baseline design vs processor+accelerator alternative design. Be sure to discuss area and cycle time before discussing the total execution time in ns and the energy for your evaluation program. Do not just discuss the results but dive into what these results mean and why each design achieves those results. Why does one design have more area? Why does one design have better performance?

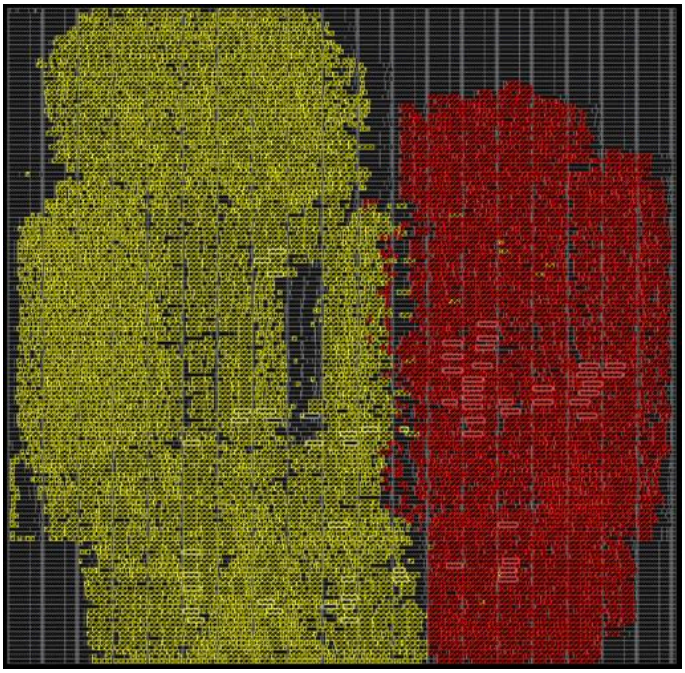
2. Accelerator Block-Level Results

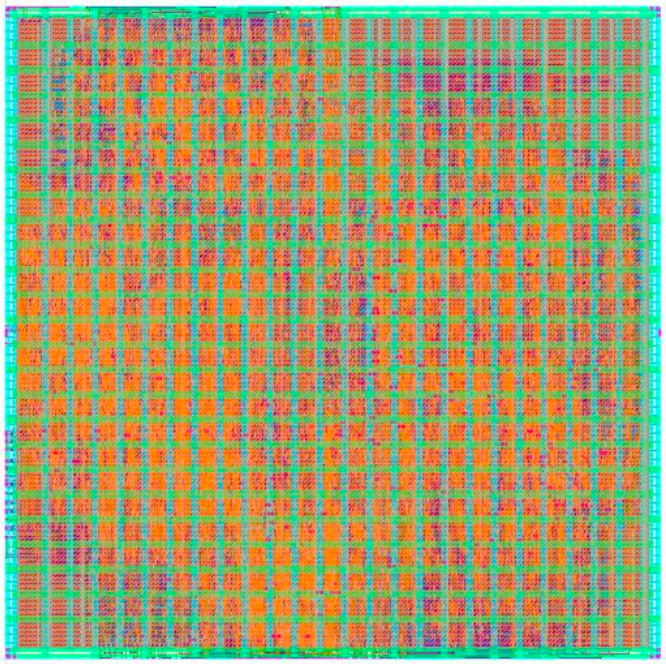




```
timestamp           = 2026-03-24 21:48:43
design_name         = GcdXcel_noparam
clock_period        = 3.0
vcs-rtlsim          = 18/18 passed
synth_setup_slack   = 0.3217 ns
synth_num_stdcells  = 461
synth_area          = 9112.275 um^2
ffglsim             = 18/18 passed
pnr_setup_slack     = 0.0442 ns
pnr_hold_slack      = 0.0132 ns
pnr_clk_ins_src_lat = 0 ns
pnr_density         = 58.34%
pnr_num_stdcells    = 527
pnr_cell_area       = 10146.214 um^2
pnr_core_area       = 18286.016 um^2
sta_setup_slack     = 0.0500 ns
sta_hold_slack      = 0.0140 ns
baglsim             = 18/18 passed
main_drc_results    = no violations found
antenna_drc_results = no violations found
lvs                 = no violations found

GcdXcel_noparam_gcd-xcel-sim-rtl-random
 - exec_time = 3220 cycles
 - exec_time = 9660.0000 ns
 - power     = 2.0170 mW
 - energy    = 19.4842 nJ

GcdXcel_noparam_gcd-xcel-sim-rtl-small
 - exec_time = 458 cycles
 - exec_time = 1374.0000 ns
 - power     = 2.9820 mW
 - energy    = 4.0973 nJ

GcdXcel_noparam_gcd-xcel-sim-rtl-zeros
 - exec_time = 157 cycles
 - exec_time = 471.0000 ns
 - power     = 3.2430 mW
 - energy    = 1.5275 nJ
```

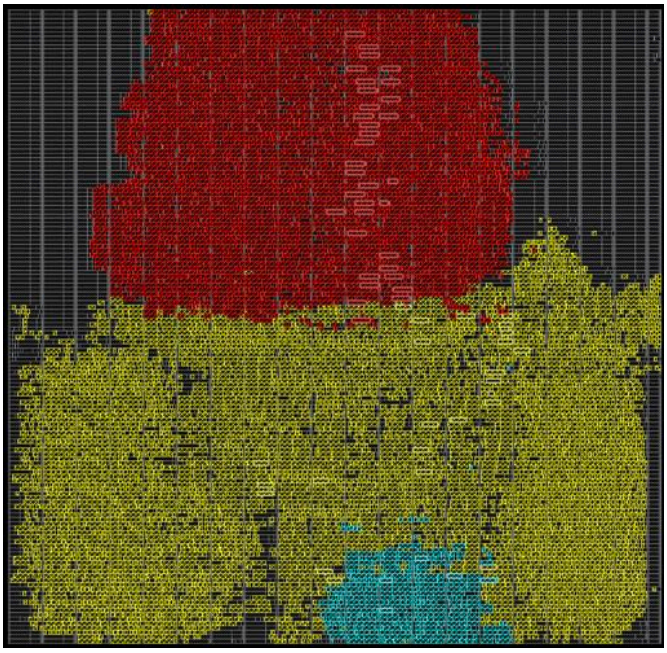
3. Processor Baseline Design Results

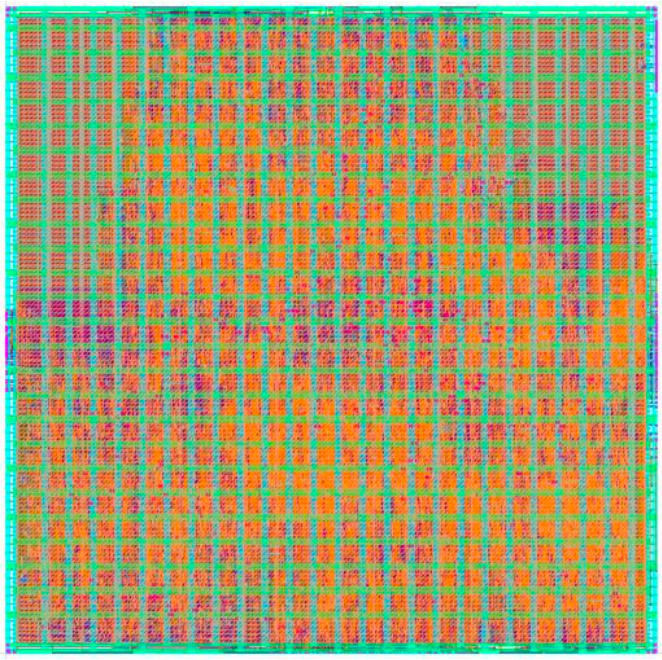




```
timestamp           = 2026-03-24 22:11:24
design_name         = ProcMemXcel_v0_NullXcel
clock_period        = 10
vcs-rtlsim          = 2/2 passed
synth_setup_slack   = 0.0275 ns
synth_num_stdcells  = 7941
synth_area          = 160012.519 um^2
ffglsim             = 2/2 passed
pnr_setup_slack     = 0.0146 ns
pnr_hold_slack      = 0.0143 ns
pnr_clk_ins_src_lat = 0 ns
pnr_density         = 64.31%
pnr_num_stdcells    = 10333
pnr_cell_area       = 197805.082 um^2
pnr_core_area       = 320218.214 um^2
sta_setup_slack     = 0.0391 ns
sta_hold_slack      = 0.0104 ns
baglsim             = 2/2 passed
main_drc_results    = no violations found
antenna_drc_results = no violations found
lvs                 = no violations found

ProcMemXcel_v0_NullXcel_pmx-sim-null-rtl-ubmark-gcd-eval
 - exec_time = 3417 cycles
 - exec_time = 34170.2080 ns
 - power     = 17.2000 mW
 - energy    = 587.7276 nJ
```

4. Processor+Accelerator Alternative Design Results





```
timestamp           = 2026-03-24 22:33:31
design_name         = ProcMemXcel_v0_GcdXcel
clock_period        = 10
vcs-rtlsim          = 2/2 passed
synth_setup_slack   = 0.0363 ns
synth_num_stdcells  = 8168
synth_area          = 164631.220 um^2
ffglsim             = 2/2 passed
pnr_setup_slack     = 0.0243 ns
pnr_hold_slack      = 0.0114 ns
pnr_clk_ins_src_lat = 0 ns
pnr_density         = 64.00%
pnr_num_stdcells    = 10591
pnr_cell_area       = 202663.059 um^2
pnr_core_area       = 329473.178 um^2
sta_setup_slack     = 0.0495 ns
sta_hold_slack      = 0.0054 ns
baglsim             = 2/2 passed
main_drc_results    = no violations found
antenna_drc_results = no violations found
lvs                 = no violations found

ProcMemXcel_v0_GcdXcel_pmx-sim-gcd-rtl-ubmark-gcd-xcel-eval
 - exec_time = 1037 cycles
 - exec_time = 10370.1810 ns
 - power     = 11.8000 mW
 - energy    = 122.3681 nJ
```